REMARKS

Claims 1 - 28 are pending in the application. Claims 12 - 19 are allowed. Claims 1, 2, 20 and 21 are rejected. Claims 3 - 11 and 22 - 28 are objected to as being dependent upon a rejected claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1, 3, 5, 8, 20, 22, 24 and 25 have been amended. For the reasons discussed below, Applicant respectfully requests for allowance of claims 1 - 11 and 20 - 28 as well.

Allowable Subject Matter

Claims 3-11 and 22-28 have been written in independent form including all of the limitations of the base claim and any intervening claims. Thus, claims 3-11 and 22-28 are now in condition of allowance.

The Rejections under 35 U.S.C. §102

Claims 1-2 and 20-21 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,923,193 to Bloch et al. (hereinafter referred to as "Bloch"). Applicant respectfully traverses the Examiner's position for the following reasons.

The independent claim 1 is directed to a signal synchronizing circuit for prohibiting signals traveling from a first clock domain operating with a first clock to a second clock domain operating with a second clock when the first clock is not active. The signal synchronizing circuit includes a detection circuit producing a detection signal indicating that the first clock is active, and at least one output selection module for passing a selected signal from the first clock domain to the second clock domain only when the detection signal indicating that the first clock is active.

According to a telephonic interview with Examiner Luu on July 8, 2005, the Examiner indicated that while Bloch does not teach "a detection circuit producing a detection signal indicating that the first clock is active," the independent claim 1 is still not allowable because the detection circuit is not properly connected with other elements of the claimed invention. In view of the foregoing, Applicant has amended claim 1 to include at least one output selection module for passing a selected signal from the first clock domain to the second clock domain only when **the detection signal** indicating that the first clock is active. The output selection module responds to the detection signal that is produced by the detection circuit. The detection signal properly connects the detection circuit and the output selection module to one anther.

As such, the independent claim 1 is now in a proper form, and patentably distinguishable over the cited prior art reference. For the same reason, the independent claim 20 is patentable over the cirted art. Claims 2 and 21 that depend on claims 1 and 20, respectively, are therefore patentable as well.

CONCLUSION

Applicant has made an earnest attempt to place this application in an allowable form. In view of the foregoing remarks, it is respectfully submitted that the pending claims are drawn to a novel subject matter, patentably distinguishable over the prior art of record. The Examiner is therefore, respectfully requested to reconsider and withdraw the outstanding rejections.

Should the Examiner deem that any further clarification is desirable, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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